

Implementation of High Speed and Low Area Confined Multiplier Using Multiplexer Based Full Adder on Fpga

K.Venkanna, M. Hari Krishna, Ch. Gopala Krishna

Associate professor, Department of Electronics and communication engineering, Sree Vahini institute of science & Technology, Tiruvuru, Krishna District, AP, India

Professor, Department of Electronics and communication engineering, Sree Vahini institute of science & Technology, Tiruvuru, Krishna District, AP, India

Associate professor, Department of Electronics and communication engineering, Sree Vahini institute of science & Technology, Tiruvuru, Krishna District, AP, India

ABSTRACT: Our project presents a comparative study of serial multiplier and advanced multiplier by using RTL simulation and Field Programmable Gate Array (FPGA) implementation. Multiplier plays a prominent role in Digital Signal Processing (DSP) applications. By changing the performance of the multiplexer performance of the applications varies. In this project many of the single bit adders are reduced and replaced by multiplexers. So that the lower utilized FPGA's are utilized fully by occupying less number of divisions and slices. Significantly reduction of FPGA resources, delay, area and power are achieved by using confined Wallace multiplier design. These multiplication techniques are designed by using RTL simulation and it is simulated in Xilinx ISE simulator and synthesis is done in Xilinx ISE 14.7. At last the design is implemented in Spartan 3E FPGA.

KEYWORDS: Wallace tree multiplier, CSLA, CSA, Xilinx, FPGA.

I. INTRODUCTION

The thirst of taking the technology to more and more heights has inculcated numerous techniques and designs which are very fast and compact than the previous technology. As the VLSI field is moving towards more compact design with higher performance, the need to develop the components which are compatible with the advancement becomes mandatory. Multiplier is the logic device of great concern in terms of performance of a processor. In any system, the task of processor is very crucial. The task that took most of the processor's time is multiplication thus enhancing the performance of multiplier leads to better performance of processor especially in field of digital signal processing and data processing ASIC. This paper work presents two different form of Wallace tree multiplier using two different adder circuits namely carry look-ahead adder and carry select adder. After developing these two different forms of Wallace tree multiplier a comparative study is being carried out on the basis of area and power consumption by the two designs. As the component size on chip is reducing to offer mobility, the dissipation of power becomes a matter of concern. Multiplication at its basic can be defined as the process of adding a number to itself a number of times. Thus it can be interpreted from this fact that addition is a sub-process in multiplication criterion that has to be fulfilled. In the process the Wallace tree formation aligned the partial products in form of a tree and then with the help of fast adders final product is obtained. After the architecture design and comparison the final step is FPGA implementation.

Adder

Adder can be defined as the functional block used for addition of numbers. The adders which will be discussed in this paper are binary adders which do the addition of binary numbers only. The basic adders are: half adder and full adder. With the help of these basic adders more complex Carry Select Adder are designed.

Carry Select Adder

The practice of addition with carry select addition approach conventionally divides the adder into blocks. If the adder is an n-bit adder and we want to divide it into blocks having m-bits each then obviously the numbers of blocks thus formed are n/m blocks. These n/m blocks performs addition of m-bits using any of the adder algorithm such as ripple

carry adder, carry skip adder, carry look-ahead adder etc. to produce the output sum and carry signals. Now the n/m blocks in the CSLA may be viewed as n/m stages consists of two m -bits adder and one m -bit 2-to-1 multiplexer each except the block in the initial stage contains the least significant bits of the two. The remaining blocks perform the addition two times, one with carry-in equals to 1 and other with the carry-in equals to 0. Then these pre-calculated values of sum bits with their respective pre-assumed carry-in values are stored in the block and when the true carry-in value becomes available, the correct pair is extracted. Now the task of the selection of the proper pair is achieved with the help of 2- to-1 MUX. The actual carrying signal acts as the select line of the MUX.

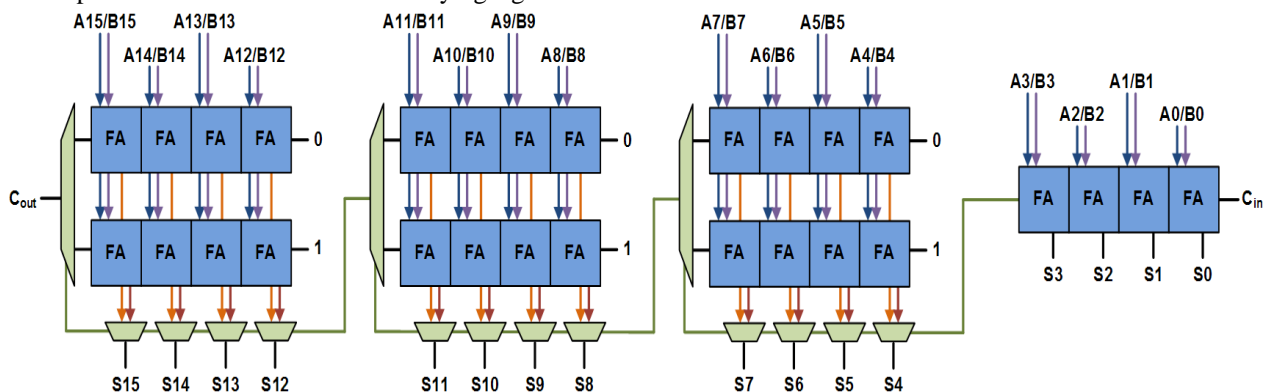


Figure 1: Carry Select Adder

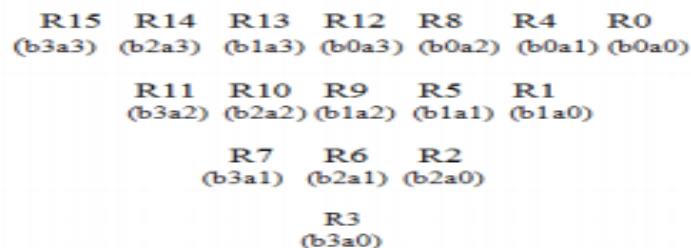
Multiplier

Multiplier is the functional device which is used to multiply two numbers. In the process of multiplication each bit of multiplier is multiplied with each bit of multiplicand and partial products are obtained. Then these partial products are added to get the final product. There are mainly two types of multipliers: array multiplier and tree multiplier. In this paper one of the tree multiplier is discussed known as Wallace tree multiplier.

Wallace Tree Multiplier

This architecture helps in reducing the partial products with a rate of $\log_3/2 N/2$. The three main steps in the algorithm of Wallace tree multiplier design are:

- 1) The multiplication of the multiplier bits with the multiplicand generates a bit product stream.
- 2) The bit product matrix thus formed has been reduced into less number of rows with the help of half and full adders, this step persists till the last addition is done.
- 3) Last and final step is the final addition using adders and the final result can be obtained after this step.



II. PROPOSED METHODOLOGY

The work presented in this dissertation report proposed the design of Wallace tree multiplier with two different architectures. In one of the architectures the Wallace tree is used with the carry select adder and in the other one it is implemented in combination of carry look-ahead adder. Then a comparative study is also shown in respect of area and power consumption. The final objective of the thesis is the hardware implementation of the proposed design. The hardware implementation is achieved on the FPGA Spartan 3e device with Xilinx atmosphere and the programming in VHDL is developed in MODELSIM. The three main steps followed in the approach suggested in the thesis are:

- Generating the partial products.

International Journal of Advanced Research in Science, Engineering and Technology

Vol. 6, Special Issue , August 2019

International Conference on Recent Advances in Science, Engineering, Technology and Management at Sree Vahini Institute of Science and Technology-Tiruvuru, Krishna Dist, A.P

- Wallace tree implementation using the partial products with half and full adders.
- Final summation using Carry select adder (CSLA).

When the proposed architectures are designed successfully then with the help of mapping report we can find out the area and power consumption and can compare which architecture provides favorable results.

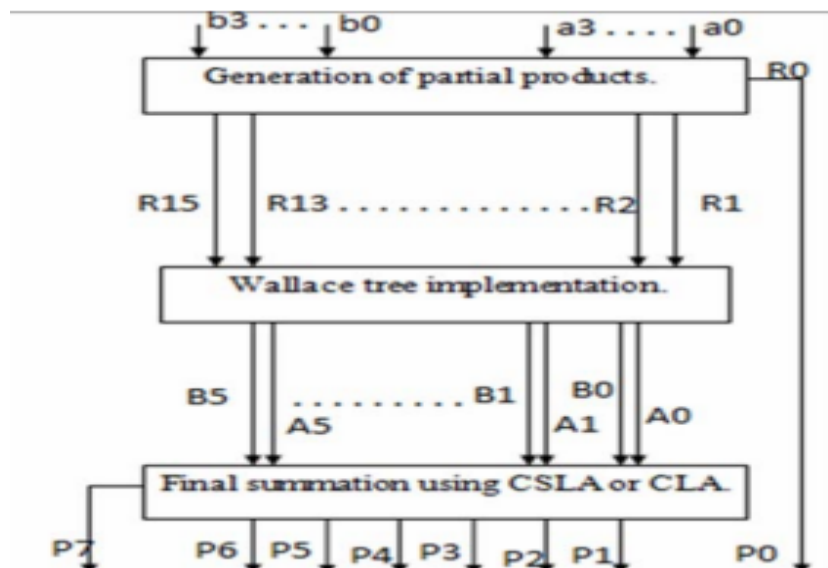


Figure 3: Design Flow of Proposed Work

In this arrangement the partial products with same weight are grouped together and written in a column. There are total six columns in the arrangement in accordance to the max weight carried by partial product term i.e. a_3b_3 has highest weight 6. Now the addition is applied in each column using half and full adder according to the need, if there are two numbers to be added then half adder is employed and if there are three numbers for addition then full adder has to be used. The main objective of Wallace tree implementation in this architecture is to generate the input terms for adders whether CSLA. As we know the first partial product a_0b_0 doesn't need any computation, it is directly taken as the LSB of the product. Therefore R_0 is equals to P_0 . Now the task we have to do is to extract two final bits from each remaining column after excluding the first column from right as it contains R_0 . Now carefully examining the columns we can see the second column from right has two partial products P_4 and P_1 , which means it has only two bits in all so they can be taken directly and termed as A_0 and B_0 . Moving further to the next column we are having three terms with us P_8 , P_5 and P_2 , so here we need to apply adders to get final two bits for CSLA. A half adder is applied with p_8 and P_5 as inputs which gives two outputs sum and carry, now from this column the sum obtained is taken as B_1 , the partial product term P_2 as A_1 and the carry so obtained as A_2 . Going ahead in this manner, we will get final six pairs of bits as A_0B_0 , A_1B_1 , A_2B_2 , A_3B_3 , A_4B_4 , and A_5B_5 . These numbers so obtained can be treated as two input numbers for the adder. The Wallace tree implementation and the adder stage can be shown in figure below.

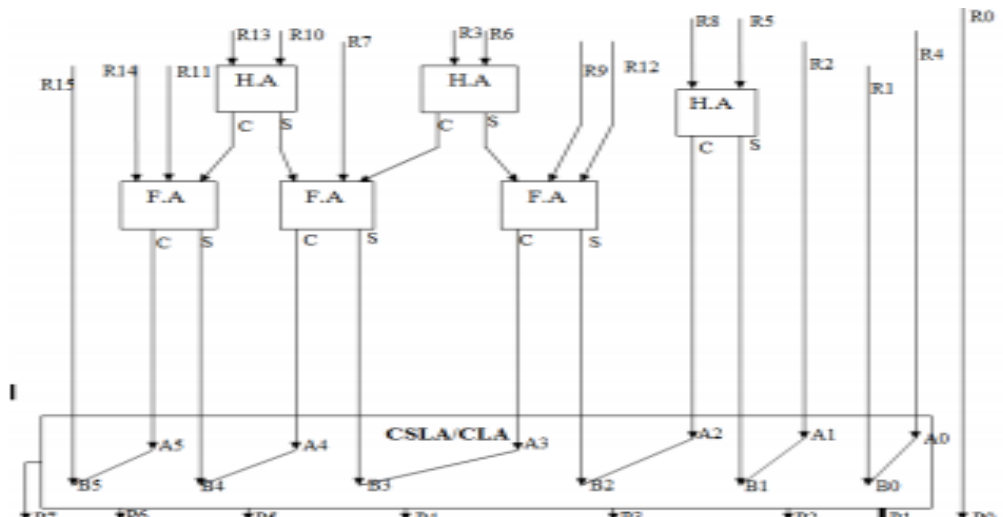
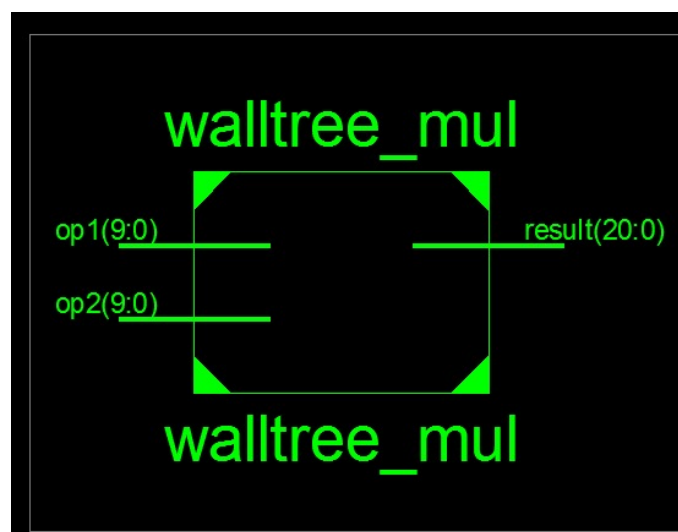


Figure 5: Wallace Tree Multiplier Using CSLA

After the Wallace tree implementation, the last step remains is the addition of the bits obtained. Through Wallace tree computation process, we obtain total 12 bits which can be divided into two numbers A (A0, A1, A2, A3, A4, A5) and B (B0, B1, B2, B3, B4, B5). Now the product of the numbers (a) and (b) can be obtained by adding numbers A and B. the LSB of the product is already known which nothing but R0 is. So $P_0 = R_0$. Now the summation of A and B will provide the remaining bits of the product. The sum bits at each stage are the product bits and the carry go to the next stage. And the final carry out is the MSB of the product. Hence, we get p1, p2, p3, P4, p5, P6 and p7 after the last step. The final step of the presented work is the hardware implementation of the multiplier design proposed in this paper on FPGA Spartan 3E. The programming is done in VHDL and with the help of Xilinx tool the code is burnt into the FPGA kit. The Simulation is done in both Xilinx environment. The area and power analysis are conducted using FPGA implementation.

Results



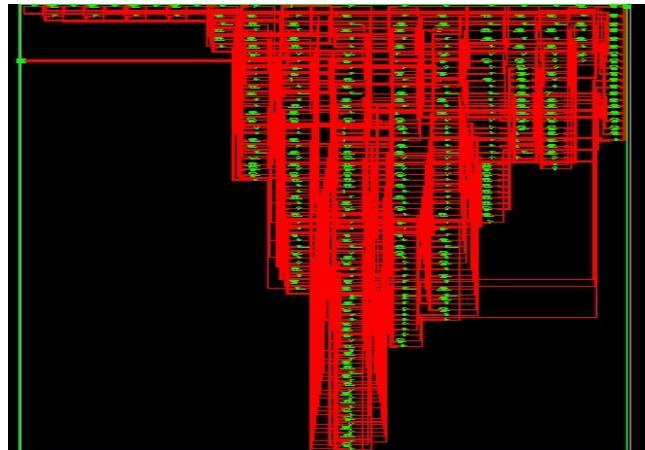


Figure 6: RTL Schematic of Wallace tree multiplier using CSLA

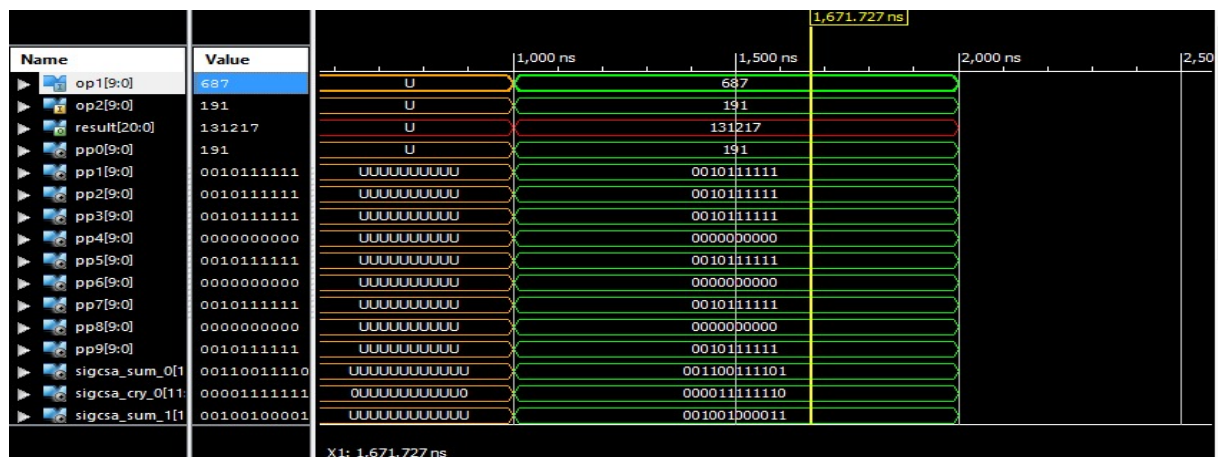


Figure 7: Output waveform for Wallace tree multiplier using CSLA

Parameters

Area

International Journal of Advanced Research in Science, Engineering and Technology

Vol. 6, Special Issue , August 2019

International Conference on Recent Advances in Science, Engineering, Technology and Management at Sree Vahini Institute of Science and Technology-Tiruvuru, Krishna Dist, A.P

Device Utilization Summary				
Logic Utilization	Used	Available	Utilization	Note(s)
Number of 4 input LUTs	249	9,312	2%	
Number of occupied Slices	139	4,656	2%	
Number of Slices containing only related logic	139	139	100%	
Number of Slices containing unrelated logic	0	139	0%	
Total Number of 4 input LUTs	249	9,312	2%	
Number of bonded IOBs	41	232	17%	
Average Fanout of Non-Clock Nets	3.05			

Delay

Total 24.773ns (15.291ns logic, 9.482ns route)
(61.7% logic, 38.3% route)
=====

Total REAL time to Xst completion: 30.00 secs
Total CPU time to Xst completion: 29.49 secs

Power

A	B	C	D	E	F	G	H	I	J	K	L	M	N
Device		On-Chip	Power (W)	Used	Available	Utilization (%)			Supply	Summary	Total	Dynamic	Quiescent
Family	Spartan3e	Logic	0.000	249	9312	3			Source	Voltage	Current (A)	Current (A)	Current (A)
Part	xc3s500e	Signals	0.000	269	---	---			Vccint	1.200	0.026	0.000	0.026
Package	fg320	IOs	0.000	41	232	18			Vccaux	2.500	0.018	0.000	0.018
Temp Grade	Commercial	Leakage	0.081						Vcco25	2.500	0.002	0.000	0.002
Process	Typical	Total	0.081										
Speed Grade	-5												
Environment		Thermal Properties	Effective TJA	Max Ambient	Junction Temp				Supply Power (W)		Total	Dynamic	Quiescent
Ambient Temp (C)	25.0		(C/W)	(C)	(C)						0.081	0.000	0.081
Use custom TJA?	No												
Custom TJA (C/W)	NA												
Airflow (LFM)	0												
Characterization													
PRODUCTION	v1.2.06-23-09												

International Journal of Advanced Research in Science, Engineering and Technology

Vol. 6, Special Issue , August 2019

International Conference on Recent Advances in Science, Engineering, Technology and
Management at Sree Vahini Institute of Science and Technology-Tiruvuru, Krishna Dist, A.P

Analysis and Future Scope

There is no doubt left in the fact that multipliers can be considered as the backbone of the processors especially in digital signal processing. As we have passed through the entire thesis, we are now capable of seeing the scope and implementation of the Digital Multipliers especially Wallace tree multiplier. The thesis elaborates all the vital parts of the design such as adders both conventional and fast adders and multipliers with all their types. This finally makes the ground for our thesis and also makes its understanding simpler. The need to develop better and optimized architectures of multipliers has led the journey of multiplier development further and further towards more profitable designs. The design propounded in this thesis is developed keeping in mind all the constraints present in today's era of technology. The main focus is given to generate the design which is hardware implemental and also consumes less area and power. As area and power factors are the burning demands for the upcoming designs, they have to be considered and analyzed. Therefore we can conclude by looking upon the area and power report so obtained that which architecture is better among the two suggested architectures which come out to be the architecture of Wallace tree multiplier using carry select adder.

III.CONCLUSION

The analysis of the multiplier architectures designed in this paper work on the basis of the area and power consumption reveals the fact that the Wallace tree multiplier using carry select adder is better in terms of both area and power consumption, which can easily be seen in the comparison tables. In this paper, several types of Wallace multiplier architectures are studied and compared with the conventional Wallace multiplier architecture. It is observed that with reduced complexity and use of efficient adders, Wallace multiplier architecture gives better performance in terms of power, delay and area.

REFERENCES

1. Wallace, C. S., "A Suggestion for a Fast Multiplier", IEEE Transactions on Computers, vol. 13, pp. 14-17, 1964.
2. Kumar, M., Hussain, M. A., and Paul, S. K., "Performance of a Two Input Nand Gate Using Subthreshold Leakage Control Techniques", Journal of Electron Devices, Vol. 14, pp. 1161-1169, 2012.
3. Kumar, M., Hussain, M. A., and Singh, L. K., "Design of a Low Power High Speed ALU in 45nm Using GDI Technique and Its Performance Comparison", Communications in Computer and Information Science, Springer Berlin Heidelberg, Vol. 142, pp. 458-463, 2011.
4. Gandhi, D. R., and Shah, N. N., "Comparative Analysis for Hardware Circuit Architecture of Wallace Tree Multiplier", IEEE International Conference on Intelligent Systems and Signal Processing, Gujarat, pp. 1-6, 2013.
5. Swartzlander, E. E., and Waters, R. S., "A Reduced Complexity Wallace Multiplier Reduction", IEEE Transactions on Computers, vol. 59, pp. 1134-1137, 2010.
6. Vinoth, C., Bhaaskaran, V. S. K., Brindha, B., Sakthikumaran, S., Kavinilavu, V., Bhaskar, B., Kanagasabapathy, M., and Sharath, B., "A Novel Low Power and High Speed Wallace Tree Multiplier for RISC Processor", IEEE 3rd International Conference on Electronics Computer Technology, Kanyakumari, pp. 330 – 334, 2011.
7. Dubey, S., and Rao, M. J., "A High Speed and Area Efficient Booth Recoded Wallace Tree Multiplier for fast Arithmetic Circuits", IEEE Asia Pacific Conference on Postgraduate Research in Microelectronics & Electronics, Hyderabad, pp. 220 – 223, 2012.
8. Sureka, N., Porselvi, R., and Kumuthapriya, K., "An Efficient High Speed Wallace Tree Multiplier", IEEE International Conference on Information Communication and Embedded system, Chennai, pp. 1023-1026, 2013.
9. Khan, S., Kakde, S., and Suryawanshi, Y., "VLSI Implementation of Reduced Complexity Wallace Multiplier Using Energy Efficient CMOS Full Adder", IEEE International Conference on Computational Intelligence and Computing Research, Coimbatore, pp. 1-4, 2013.